Journal of Electroceramics 4:2/3, 339–344, 2000

The Mott Transition Field Effect Transistor: A Nanodevice?

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Abstract. A field effect transistor device (FET), consisting of a nonlinear Mott Insulator channel material, and a high dielectric-constant gate oxide, is explored as a nanoscale device. Experimental functionality of a large scale prototype (5 μm channel length) has been demonstrated. The underlying physics of the device is analyzed and modeled using a time-dependent Hartree approach. Timing estimates suggest a relatively short switching time.

Keywords: FET, field effect, ferroelectric, Moore's law, nanoscale, Mott, perovskite

1. Introduction

For over a decade the linear feature size of silicon microcircuits has decreased exponentially with time, with a corresponding near-exponential increase in circuit density on a chip (Moore's law). However, the key circuit element, the metal oxide semiconductor field effect transistor (MOSFET), is approaching the intrinsic physical limits of channel length (about 50–60 nm [1]) for the standard scaled device formed with an SiO_2 gate insulator. In the next couple of years further miniaturization will require modification of the gate oxide material [1,2] and, from this point on, increasingly radical materials/design changes will be required to achieve additional scale reductions.

In this paper we explore a global redesign concept of the field effect transistor whose objective is functionality at the 10 nm channel length scale, assuming that such scales will eventually be achievable by future manufacturing technology advances. The approach is first to abandon the bulky source-channel and drain-channel $p-n$ junctions of the MOSFET, whose presence underlies its excellent ''turn off'' characteristics, working instead with a majority carrier device. The concept replaces the silicon channel by an intrinsically nonlinear conducting material, the Mott Insulator, discussed in more detail below. An adequate ''on'' conductance is achieved by means of a high ''on'' carrier density, which induces a gradual Mott transition in the normally insulating channel toward a conducting, metallic, state. The short screening length in the metallic state—conveniently for scaling purposes—confines the channel below ~ 1 nm thickness. A high dielectric–constant gate oxide is required to achieve sufficient carrier density at ~ 1 V on the gate. It is expected that the potentially serious boundary scattering problem in such a thin channel can be mitigated by building the device with an epitaxial interface between the gate oxide and channel materials.

2. Principles of Operation

The device concept, termed the Mott transition field effect transistor (MTFET) [3,4], due to the role played by the channel nonlinearity, is sketched in Fig. 1. The electrode configuration, involving source, drain and gate electrodes, is similar to that in the MOSFET. The channel material consists of a suitable Mott insulator. The gate oxide is relatively thick, which is acceptable (see below) for a high dielectric-constant ferroelectric type material. The gate oxide/channel interface is epitaxially grown.

Comparison at the microscopic level between the semiconducting and Mott insulator materials is illustrated in Fig. 2. In the semiconductor (top panel), a qualitatively correct picture is that the

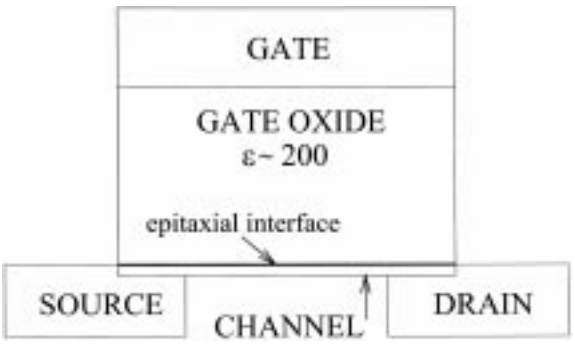

Fig. 1. Sketch of the MTFET concept. The source and drain electrodes are separated by a channel consisting of a nonlinear Mott Insulator material. The gate oxide is fabricated from a high dielectric-constant material. The gate oxide/channel interface is epitaxial.

electrons bound in pairs in the Si:Si bonds form the valence band with 4 electrons per Si atom. The gap in the Si band structure is in some sense associated with the bonding→antibonding excitation energy of the Si bond. However, in the typical Mott insulator [5] (center panel), electrons are bound 1:1 to the 3d transition metal atoms. This happens because in the compact 3d orbitals, the intra-atomic electron-electron Coulomb repulsion U is large, and the inter-atomic hopping energy t_h is low. Hence, the electron binding site is surrounded by a Coulomb barrier U due to the energy cost of a double site occupation, which is insurmountable by the hopping kinetic energy because $U \gg t_h$. Interestingly, this is Coulomb blockade electron localization similar to that in a quantum dot array. The condition $U \gg t_h$ is the same one as that restricting the inter-dot conductance to less than one quantum of conductance in order for the Coulomb blockade to occur.

The lower panel in Fig. 2 illustrates the metallization of the Mott insulator by hole doping [5]. The availability of empty sites enables hopping of electrons between sites without incurring the energy penalty U. As the concentration of holes increases, the enhancement of the intersite hopping processes leads to the disappearance of the Coulomb Blockade gap, when the system can be thought of as a metal.

In the ''off'' state, the relatively wide Mott insulator gap (1–2 eV) should ensure, at 1 V drain potential, that there is a potential barrier accross all or most of the width of the channel (see Fig. 2 in [3]).

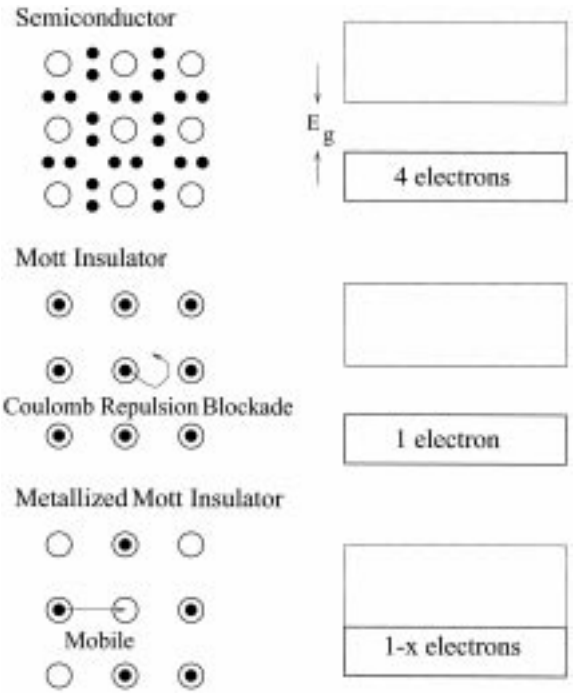

Fig. 2. Top panel: bonds and bands in Si. Center panel: electron binding to atoms in Mott insulator, with resulting energy gap above band with single electron per site. Lower panel: metallization of Mott insulator by hole doping, with loss of energy gap.

Hence, the MTFET channel should be insulating under these conditions.

3. Choice of Materials

The cuprate materials related to high temperature superconductors are well researched Mott insulators [5] which, upon hole doping, become p-type conductors. These materials can form epitaxial interfaces with ferroelectric high dielectric–constant insulators such as $SrTiO_3$ (STO), and are candidate materials for a p-type MTFET device. Earlier work has also reported on superconducting and normal state oxide-channel field effects [6–9]. In Fig. 3 we display some transport data [10] for $La_{2-x}Sr_xCuO_4$ (LSCO) as a function of composition. At $x = 0$ the material is a Mott insulator. Chemically increasing hole concentration x gradually metallizes the material (Fig. 2). Unlike Si, conductivity increases faster than linearly with hole concentration due to the Mott transition effect (lacking reliable results for very small x, an

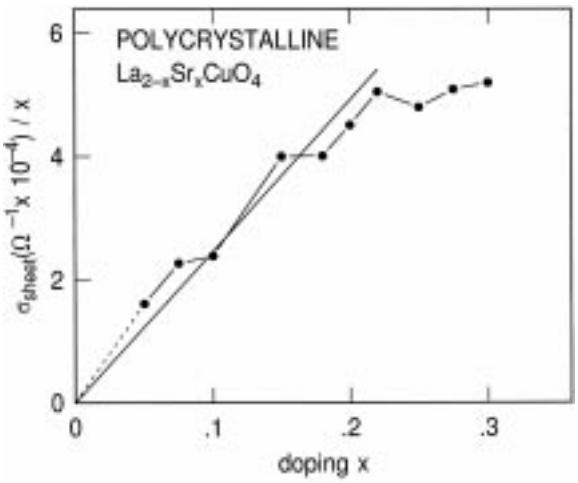

Fig. 3. Conductance per hole of $La_{2-x}Sr_xCuO_4$ (LSCO) polycrystalline samples, of various hole concentrations x per Cu, plotted as conductance per hole vs. x. Dotted line is extrapolation from lowest point to origin. Straight line is a guide to the eye.

extrapolation to zero at $x = 0$ has been included in Fig. 3, although there will be a small finite mobility at $x = 0$). The cuprate material is considered to be metallized at about $x = 0.15$, which is also a composition at which superconductivity is well established. At room temperature the sheet conductance of a single CuO_2 layer in a metalized single crystal sample of a cuprate superconductor (several times larger than that of the polycrystalline sample in Fig. 3) is comparable to that in the Si channel of a 0.1 μm channel length MOSFET [10,11].

In the MTFET, the chemical doping with holes of Fig. 3 is replaced by electrostatic induction of holes into the channel from the source and drain electrodes by application of a negative gate-to-source voltage (Fig. 4). The hole concentration per unit area of channel is approximately given by

$$N_h \sim V_g \varepsilon_{ox} \varepsilon_0 / (e d_{ox}) \qquad (1)$$

where d_{ox} and ε_{ox} are the gate oxide thickness and dielectric constant respectively, and e is electronic charge. It is possible to achieve by this means the metallic concentration $x = 0.15$ of holes within the depth of a single cuprate layer, equivalent to an area hole concentration $N_h \simeq 10^{14}\,\mathrm{cm}^{-2}$. This can be obtained with $V_g = 1\,\mathrm{V}$ if, for example, the parameters are $d_{ox} = 15\,\mathrm{nm}$, $\varepsilon_{ox} = 300$. In general, there can be a problem with fall off of dielectric constant

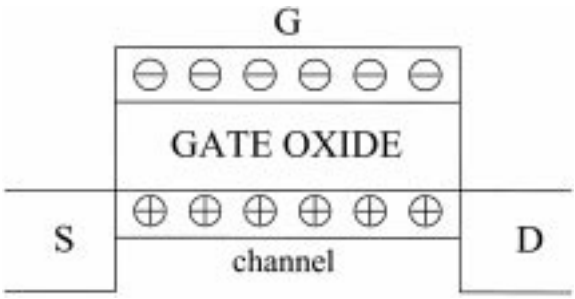

Fig. 4. Turn-on of a *p*-type MTFET by inducing flow of holes (⊕) out of source and drain electrodes into the channel via a negative potential (⊖) on the gate.

with d_{ox} in very thin layers of ferroelectric-type dielectric oxides (see [12] and references therein). However, recent work (e.g., [13]) with very thin ($d_{ox} = 20\,\mathrm{nm}$) layers of barium strontium titanate (BST) dielectric sandwiched between $SrRuO_3$ electrodes has demonstrated that it is more than possible to satisfy this metallization condition.

4. Large Scale Prototype

Our first MTFET devices have been relatively large scale (channel length of microns) devices with thick

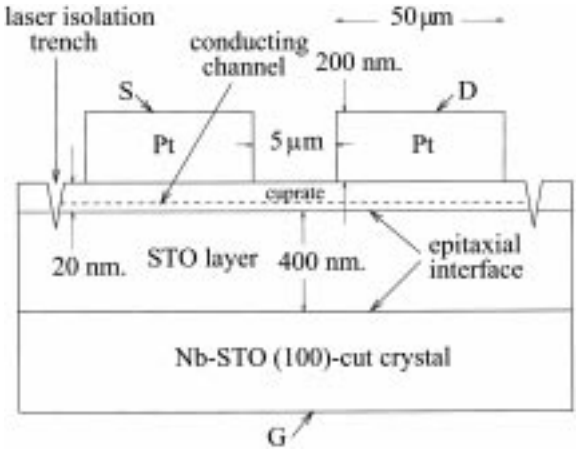

Fig. 5. Large scale MTFET device fabricated by laser deposition of STO (approx. 400 nm thickness) upon a conducting 1 atomic % Nb-STO substrate acting as the gate electrode, followed by *in situ* deposition of channel material also by laser ablation. Pt is evaporated through a contact mask to form the source and drain electrodes, followed by formation of an isolation trench via laser treatment.

ferroelectric oxide films. Figure 5 illustrates the typical device configuration employed. Starting from a 1 atomic % conducting STO substrate, which forms the gate electrode, a layer of STO gate oxide (thickness approx. 200 nm) is deposited by laser ablation. Changing targets within the laser ablation chamber, the channel material is deposited upon the STO layer. In a separate chamber, Pt electrodes forming the source and drain are evaporated through a contact mask. Finally an isolation trench in the cuprate layer is ablated out by laser treatment. We have fabricated devices from LCO, $Y_{0.5}Pr_{0.5}Ba_2Cu_3O_{7-\delta}$ (YPBCO), and from $YBa_2Cu_3O_{7-\delta}$ (YBCO). The LCO material (undoped LSCO) is a Mott insulator, as is the YPBCO. The YBCO is metallic as deposited, but by a series of annealing steps in which oxygen content is reduced, the channel material becomes again a Mott insulator [14].

We have previously published data for the YPBCO channel [4]. Here we illustrate new data for a YBCO channel, processed as mentioned above by oxygen removal to achieve a Mott insulating state [14]. Results are illustrated in Fig. 6. The YBCO devices give ON/OFF ratios as large as 2500. The carrier concentrations reached in these devices at maximum V_g are close to the desired value of 10^{14} cm^{-2} required for full metallization, but the currents achieved, although substantial, are a factor of 10–100 below those anticipated from the transport properties of metallic single crystal samples. This latter finding, not atypical of new types of FET devices, is most probably attributable to imperfect epitaxy over large scales at the gate oxide/channel interface.

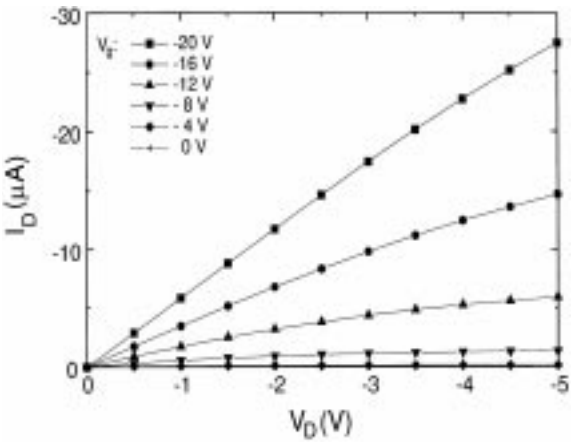

Fig. 6. Experimental drain current vs drain-to-source voltage characteristics, for various gate-to-source voltages for device of Fig. 5 with an annealed YBCO channel. Channel width 9 μm.

We have achieved an FET effect even in devices lacking a gate oxide [15]. The role of the gate oxide insulator is now played by the Schottky barrier formed at the interface between the *p*-type cuprate material and the *n*-type Nb-STO substrate. A fairly extended depletion layer is expected to be formed within the Nb-STO substrate at the interface with the cuprate, whose thickness W can be estimated to be about 40 nm from the standard formula

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_{ox}(V_b + V_g)}{eN_D}} \tag{2}$$

where V_b is the Fermi energy difference between Nb-STO and cuprate, and N_D is the Nb dopant concentration. A much thinner depletion layer should be formed within the cuprate, which has a lower dielectric constant and a larger dopant concentration than the STO.

The gate oxide-free device is fabricated on a substrate with only 0.1 atomic % Nb, and with a high quality stepped surface, in the same manner as that in Fig. 5, omitting the STO ablation step. In Fig. 7 the lower curve shows the strong variation of the drain-gate capacitance with gate voltage characteristic of a Schottky junction. The capacitance scales inversely with depletion layer thickness W, and hence a plot of C_{dg}^{-2} vs V_g should be linear, as is approximately the case in Fig. 7 (the deviations from linearity are interpretable in terms of the nonlinear STO dielectric constant measured by Christen et al. [16]). The current versus voltage curve for the junction is also Schottky Diode-like, with a rapid increase in current for V_g just beyond -1 V. Operation as a FET involves the positive gate voltage region, because the negative gate region is blocked by forward diode conduction. Hence it is only possible to *deplete* the existing carriers in the cuprate film, which is approximately 20 cuprate layers thick, by an amount of order one layer, yielding a $\sim 5\%$ effect on the conductance, as seen in the upper curve in Fig. 7 showing the drain-current versus gate-to-sources voltage characteristic. The device, which we term the Junction MTFET (JMTFET), should however perform well when very thin cuprate films having one to a few Cu layers can be uniformly fabricated, permitting good ON/OFF current ratios to be obtained.

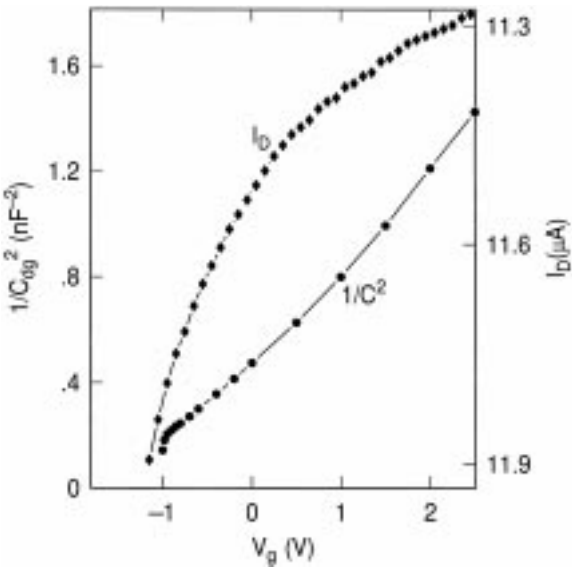

Fig. 7. Characteristics of JMTFET type device. Lower curve, plot of measured $1/C_{dg}^2$ vs. V_g showing characteristic-voltage dependent capacitance of Schottky barrier; Top curve, measured I_D vs. V_g. Device is YPBCO, channel length 5 μm, capacitance C_{dg} measured at 10 Hz, refers to isolation area approx. $200 \times 200\,\mu\text{m}^2$.

5. Quantum Simulation

We conclude with some discussion of device timing, which consists of three components: the intrinsic time for carriers to infiltrate into and out of the channel, the response time of the high dielectric–constant gate oxide, and the capacitative charging time.

Carrier motion in the channel mostly arises from the quantum kinetic energy in the degenerate electron gas, rather than from thermal motion. Only the quantum kinetic energy is large enough to overcome the localizing potential energy in the Mott insulator state: the much smaller thermal kinetic energy would not lead to full metallization.

We investigated carrier propagation microscopically by solving the time-dependent self-consistent Hartree equation for a two dimensional square lattice of atoms. The lattice dimensions were $N \times (2M + N)$ $(M > N)$, involving a central $N \times N$ section describing the channel, and $N \times M$ sections describing the source and drain electrodes. The self-energy of the electrode atomic sites is a constant set to zero; the self-energy of a channel site i is $V_c + V_i$, where V_c is the gate induced channel potential, and the Coulomb term V_i is the Coulomb potential of the charges on all other channel sites $j \neq i$, taking into consideration the dielectric constant of the channel material and the interface with the gate oxide dielectric. Interatomic electron transfer was mediated via a nearest neighbor hopping integral $t_h = <\psi_i|\mathscr{H}|\psi_j>$, where ψ_i and ψ_j are atomic orbitals on nearest neighbor atoms i and j respectively, and $\mathscr{H}$ is the Hamiltonian. The simplified model involved spinless electrons with a Hartree wavefunction

$$\Psi(t) = \Pi_{l=1}^{n_e} \psi_l(t) \tag{3}$$

which is a product of the n_e wavefunctions for each electron l in the system. A time dependent gate potential $V_c(t)$ was applied to turn on or turn off the device, and the wavefunction evolved in time according to

$$\Psi(t + dt) = e^{i\mathscr{H}(t)dt}\Psi(t) \tag{4}$$

where $\mathscr{H}(t)$ is the Hamiltonian comprising the Coulomb energy of the channel charges, t_h is the

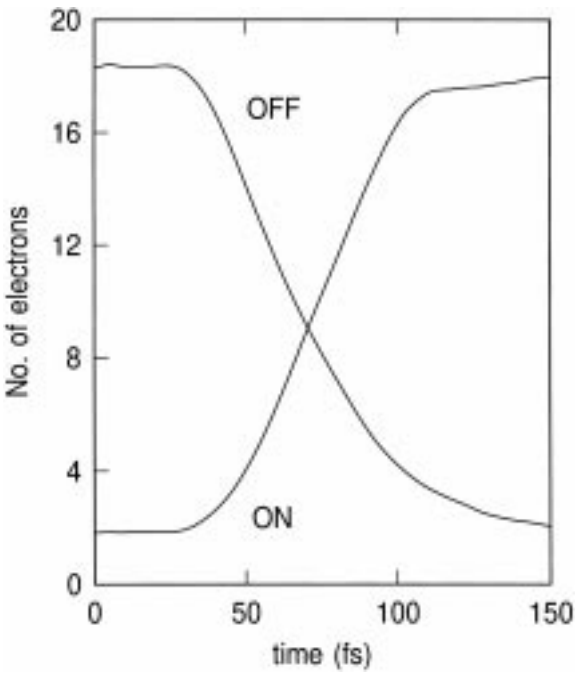

Fig. 8. Turn on and turn off of a 4 nm × 4 nm channel model device in time-dependent Hartree approximation. Parameters: $N = 10$, $M = 30$, $n_e = 150$, $t_h = -0.136$ eV, lattice spacing 8 atomic units, spacing from gate oxide surface to channel plane 8 a.u., channel dielectric constant 25. In turn on, initial $V_c = 0.27$ eV, final $V_c = -0.27$ eV, switching is linear in time over 50 fs in turn off, the potentials are reversed.

nearest neighbor hopping, and $V_c(t)$ is the gate-induced channel self-energy. Typical ON/OFF and OFF/ON switching behaviors are shown in Fig. 8 for a 10×10 channel, with a 4 nm channel length. The switching time is extremely short, 0.05 ps, and is not anticipated to increase beyond a few tenths of a picosecond for a 10 nm channel.

The dielectric response time of a ferroelectric gate oxide is determined by the soft mode phonon frequency. For STO, this number is available from neutron scattering data [17], and at 300 K is 0.35 ps.

The device capacitative charging time is likely to be dominated by the gate charge due to the high dielectric–constant gate oxide. For a $10\,\text{nm} \times 40\,\text{nm}$ cuprate channel, $(25 \times 100\,\text{Cu atoms})$ the charge is approximately 400 electrons at doping $x = 0.16$, leading at a drain current of 200 μA to a charge time of 0.3 ps. Note that this gate capacitance is roughly equivalent to about 0.3 μm of wiring.

The three estimated time delays are sub-picosecond, suggesting the feasibility of, say, 10 GHz or higher clock frequencies.

6. Concluding Remarks

At the present time, the very new MTFET concept has received a degree of experimental and theoretical support. Despite recent progress [14], a major experimental endeavour continues to be the achievement of a mobility in the MTFET that is comparable to that found in macroscopic single crystal samples. Further work needs to be done to gain an understanding of the transport mechanisms in the deep subthreshold range of operation. The feasibility of the MTFET as a practical device in densely packed integrated circuits depends upon it having a lower ''off'' (leakage) current so as to give an acceptable stand-by power. Simulations of the nanoscale MTFET [18] however appear to demonstrate adequate performance from an engineering perspective. Finally, lithogaphic techniques capable of fabricating MTFET structures on submicron scales need to be developed.

Acknowledgment

We are grateful to George Trafas for his indispensible technical assistance.

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